CARAGA STATE UNIVERSITY
Ampayon, Butuan City

Project Reference Number: 13042839

Name of Project: PROVISION OF SUBSCRIPTON EXPENSES-ICT FOR THE OPERATION OF DOST - PCIEERD - DEVELOPMENT OF DESIGN ANALYSIS AND METHODOLOGIES FOR ULTRA-LOW POWER LDO IN 5G- ADVANCED AND 6G POWER MANAGEMENT APPLICATIONS (MAY 1, 2026 - APRIL 30, 2027)

Location of Project: Caraga State University

Republic of the Philippines
CARAGA STATE UNIVERSITY
Ampayon, Butuan City 8600, Philippines
Competence Service Uprightness
PROCUREMENT OFFICE
PHONE 0917 727 8713 Loc 248 | EMAIL csuprocurement@carsu.edu.ph

NOTICE OF AWARD

Jun 15, 2026

ADVANCED COMPUTING SOLUTION, INC.
5/F Richville Corporate Tower, MBP Ayala Alabang

Dear Sir / Madam:

We are happy to notify you that the PROVISION OF SUBSCRIPTON EXPENSES-ICT FOR THE OPERATION OF DOST - PCIEERD - DEVELOPMENT OF DESIGN ANALYSIS AND METHODOLOGIES FOR ULTRA-LOW POWER LDO IN 5G- ADVANCED AND 6G POWER MANAGEMENT APPLICATIONS (MAY 1, 2026 - APRIL 30, 2027) TRF-184-26-06-164 is hereby awarded you as the bidder with the Lowest Calculated and Responsive Quotation at a Contract Price of Equivalent to ONE MILLION EIGHT HUNDRED THOUSAND PESOS ONLY. (Php 1,800,000.00)

QTY	Unit	Description	BID PRICE	TOTAL PRICE
1	LOT	ELECTRONIC DESIGN AUTOMATION (EDA) SOFTWARE TOOL (FOR INTEGRATED CIRCUITS). The bidder shall provide an Electronic Design Automation (EDA) software suite for use by academic institutions. The software shall support the complete design, simulation, verification, and analysis flow for analog, radio-frequency (RF), and mixed-signal integrated circuits (ICs). The solution shall enable transistor-level and custom integrated circuit design workflows, supporting both educational and research applications. Minimum Technical Requirements Custom IC Design and Layout Provide an integrated environment for schematic capture, circuit design, and physical layout creation. Support custom transistor-level design methodologies. Include layout productivity features such as automated or semi-automated layout assistance, constraint-driven editing, and design reuse capabilities. Circuit Simulation Provide SPICE-compatible simulation capabilities for analog, RF, and mixed-signal circuits. Support DC, AC, transient, noise, Monte Carlo, parametric sweep, and corner analysis simulations. Deliver simulation accuracy suitable for academic research and advanced IC design applications. Large-Scale and RF Analysis Support efficient simulation of large transistor-count circuits and subsystems. Provide RF and frequency-domain analysis capabilities, including support for high-frequency circuit characterization and wireless communication applications. Physical Verification Include Design Rule Checking (DRC) to verify compliance with semiconductor manufacturing process rules. Include Layout Versus Schematic (LVS) verification to ensure consistency between schematic and physical layout	1,800,000.00	1,800,000.00

P.O. # TRF-184-26-06-139

Please acknowledge receipt and acceptance of this notice by signing both copies in the space provided below, keep one copy and return the other to Caraga State University.

Very truly yours,

REDACTED

ROLYN C. BAGUL, Ph.D
University President

I acknowledge receipt of this Notice on 03 JUN 2026
Name of the Representative of the Bidder GENESIS D. OROZCO
Authorized Signature REDACTED REDACTED

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QTY	Unit	Description	BID PRICE	TOTAL PRICE
		representations. Support batch and interactive verification workflows. Parasitic Extraction and Post-Layout Analysis Provide extraction of parasitic resistance, capacitance, and, where applicable, inductance from physical layouts. Support post-layout simulation using extracted parasitic data to evaluate circuit performance under realistic operating conditions. Design Data Management and Interoperability Support industry-standard file formats and process design kits (PDKs). Provide integration capabilities between design, simulation, and verification environments. Support collaborative academic and research workflows. Licensing Requirements Provide licenses for a minimum of fifteen (15) concurrent or named users. License validity shall be for a minimum period of three (3) years. Include software updates, maintenance, and technical support during the license term.		
		xxxxxxxxx NOTHING FOLLOWS xxxxxxxx	TOTAL AMOUNT:	1,800,000.00

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